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1 [Software performance engineering a digital signal processing application](#)



David P. Kelly, Robert S. Oshana

 October 1998 **Proceedings of the 1st international workshop on Software and performance WOSP '98**

Publisher: ACM Press

 Full text available: [pdf\(889.43 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

2 [Countersniper system for urban warfare](#)



Ákos Lédeczi, András Nádas, Péter Völgyesi, György Balogh, Branislav Kusy, János Sallai, Gábor Pap, Sebestyén Dóra, Károly Molnár, Miklós Maróti, Gyula Simon

 November 2005 **ACM Transactions on Sensor Networks (TOSN)**, Volume 1 Issue 2

Publisher: ACM Press

 Full text available: [pdf\(2.77 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

An ad-hoc wireless sensor network-based system is presented that detects and accurately locates shooters even in urban environments. The localization accuracy of the system in open terrain is competitive with that of existing centralized countersniper systems. However, the presented sensor network-based solution surpasses the traditional approach because it can mitigate acoustic multipath effects prevalent in urban areas and it can also resolve multiple simultaneous shots. These unique character ...

Keywords: Sensor networks, acoustic source localization, data fusion, message routing, middleware services, time synchronization

3 [ASDEN: a comprehensive design framework vision for automotive electronic control systems](#)



Deborah Wilson, Daniel Dayton, R. Todd Hansell

 May 2000 **Proceedings of the eighth international workshop on Hardware/software codesign**

Publisher: ACM Press

 Full text available: [pdf\(55.08 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The automotive electronics industry is experiencing an era of unprecedented growth. Driven by emissions and safety legislation, fuel economy constraints, cost constraints, and customer demand for convenience features and enhanced performance, electronic controls

are steadily replacing their mechanical and hydraulic predecessors. As the sophistication of these systems grows, their complexity has grown dramatically as well, creating difficulties in the application of traditional engineering m ...

4 A VHDL compiler based on attribute grammar methodology



R. Farrow, A. G. Stanculescu

June 1989 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1989 Conference on Programming language design and implementation PLDI '89**, Volume 24
Issue 7

Publisher: ACM Press

Full text available: pdf(1.49 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents aspects of a compiler for a new hardware description language (VHDL) written using attribute grammar techniques. VHDL is introduced, along with the new compiler challenges brought by a language that extends an Ada subset for the purpose of describing hardware. Attribute grammar programming solutions are presented for some of the language challenges. The organization of the compiler and of the target virtual machine represented by the simulation kernel are disc ...

5 Hardware/software co-design: VHDL and Ada 95 code migration and integrated analysis



Mike Mills, Greg Peterson

November 1998 **ACM SIGAda Ada Letters , Proceedings of the 1998 annual ACM SIGAda international conference on Ada SIGAda '98**, Volume XVIII Issue 6

Publisher: ACM Press

Full text available: pdf(800.58 KB)

Additional Information: [full citation](#), [references](#), [index terms](#)

An automated system for creating and managing VHDL design units is described in this paper. This system helps the hardware designer to learn the syntax of the VHSIC Hardware Description Language (VHDL) and to produce code which can be used for simulations. This demonstration prototype tool is written in C to run on a Sun workstation, and it produces IEEE standard 1076 VHDL code.

6 COMP: a VHDL composition system



P. R. Jordan, R. D. Williams

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**
Publisher: ACM Press

Full text available: pdf(501.93 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

An automated system for creating and managing VHDL design units is described in this paper. This system helps the hardware designer to learn the syntax of the VHSIC Hardware Description Language (VHDL) and to produce code which can be used for simulations. This demonstration prototype tool is written in C to run on a Sun workstation, and it produces IEEE standard 1076 VHDL code.

7 The IBM VHDL design system



L. F. Saunders

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**
Publisher: ACM Press

Full text available: pdf(501.38 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents the IBM VHDL Design System. This set of Computer Aided Engineering (CAE) design tools, built around the VHSIC Hardware Description Language (VHDL) and developed for IBM internal use, along with other design automation tools, is used by IBM design engineers to develop computer hardware. The function and operation of each piece of the system is described. IBM usage and some of the problems encountered are also discussed.

8 An interface between VHDL and EDIF



M. Shahdad

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation****Publisher:** ACM Press

Full text available: pdf(749.85 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The VHSIC Hardware Description Language (VHDL) and the Electronic Design Interchange Format (EDIF) are becoming industry standards for hardware design and documentation. Potential users of these standards are interested in understanding the application range of each standard and the way each standard relates to the other. This paper presents scenarios in which VHDL and EDIF can contribute to different aspects of the design process, as well as the technical issues in providing a design inter ...

9 VHDL teamwork, organization units and workspace management

S. Olcoz, L. Ayuda, I. Izaguirre, O. Penalba

February 1998 **Proceedings of the conference on Design, automation and test in Europe****Publisher:** IEEE Computer Society

Full text available: pdf(96.44 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)[Publisher Site](#)

A new set of tools for Teamwork, Organization Units, Workspace and Build management of VHDL-based reusable components, organized in libraries, accessible through an heterogeneous and distributed environment is presented. These tools support the collaborative and distributed development of systems-on-a-chip reusing VHDL components available through the intranets and the Internet. They must be used as a complementary support to the design tools (simulation, synthesis, etc.) already available in th ...

Keywords: Teamwork, cooperative work, workspace, management, VHDL analysis, elaboration, simulation.

10 A VHDL error simulator for functional test generation



Alessandro Fin, Franco Fummi

January 2000 **Proceedings of the conference on Design, automation and test in Europe****Publisher:** ACM Press

Full text available: pdf(72.38 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)[Publisher Site](#)

11 Translation of VHDL to Ada

Carl F. Schaefer

March 1987 **Proceedings of the Joint Ada conference fifth national conference on Ada technology and fourth Washington Ada Symposium****Publisher:** George Washington University

Full text available: pdf(521.08 KB)

Additional Information: [full citation](#), [references](#), [index terms](#)

12 An overview of VHDL language and technology

Moe Shahdad

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation****Publisher:** IEEE PressAdditional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Full text available:  [pdf\(812.50 KB\)](#)[terms](#)

VHDL language and technology has been under development for the past five years, resulting in a hardware description language that enjoys widespread support within the industry. Version 7.2 of the language was released in August of 1985 and is being considered by the IEEE as a prime candidate for standardization. It is expected that a proposed standard based on Version 7.2 will be available in January of 1987. This standard will be accompanied by a VHDL Tutorial containing extensive example ...

13 [Reasoning about VHDL and VHDL-AMS using denotational semantics](#)



P. T. Breuer, N. Martinez Madrid, J. P. Bowen, R. France, M. Lorrondo Petrie, C. Delgado Kloos

January 1999 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: ACM Press

Full text available:  [pdf\(488.86 KB\)](#) Additional Information: [full citation](#), [citations](#), [index terms](#)

14 [The role of VHDL in the MCC CAD system](#)



Ramón D. Acosta, Mark Alexandre, Gary Imken, Bill Read

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Publisher: IEEE Computer Society Press

Full text available:  [pdf\(753.39 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The VHSIC Hardware Description Language (VHDL), currently undergoing standardization by the IEEE, supports the hierarchical design, documentation, and simulation of a wide range of digital system abstractions. This paper describes a suite of utilities for manipulating VHDL designs that has been developed and integrated into the CAD System of the Microelectronics and Computer Technology Corporation (MCC). The MCC CAD System is a tightly integrated environment supporting the sharing of design ...


15 [A refinement calculus for the synthesis of verified hardware descriptions in VHDL](#)



Peter T. Breuer, Carlos Kloos Delgado, Andrés López Marín, Natividad Martínez Madrid, Luis Sánchez Fernández

July 1997 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 19 Issue 4

Publisher: ACM Press

Full text available:  [pdf\(392.21 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A formal refinement calculus targeted at system-level descriptions in the IEEE standard hardware description language VHDL is described here. Refinement can be used to develop hardware description code that is "correct by construction". the calculus is closely related to a Hoare-style programming logic for VHDL and real-time systems in general. That logic and a semantics for a core subset of VHDL are described. The programming logic and the associated refinement calculus are sh ...

Keywords: VHDL, denotational semantics, digital circuits, formal verification, program logic, refinement, timed logic

16 [VHDL development system and coding standard](#)



Hans Sahm, Claus Mayer, Jörg Pleickhardt, Johannes Schuck, Stefan Späth

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Publisher: ACM Press

Full text available:  pdf(147.15 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

17 BDD-based testability estimation of VHDL designs



E. Macii, M. Poncino, F. Ferrandi, F. Fummi, D. Sciuto

September 1996 **Proceedings of the conference on European design automation**

Publisher: IEEE Computer Society Press

Full text available:  pdf(308.06 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

18 A VHDL reuse workbench



G. Lehmann, K. Müller-Glaser, B. Wunder

September 1996 **Proceedings of the conference on European design automation**

Publisher: IEEE Computer Society Press

Full text available:  pdf(301.67 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

19 An effective system development environment based on VHDL prototyping



Serafín Olcoz, Luis Entrena, Luis Berrojo

December 1995 **Proceedings of the conference on European design automation**

Publisher: IEEE Computer Society Press

Full text available:  pdf(685.32 KB) Additional Information: [full citation](#), [references](#), [index terms](#)

20 Inheritance concept for signals in object-oriented extensions to VHDL



Guido Schumacher, Wolfgang Nebel

December 1995 **Proceedings of the conference on European design automation**

Publisher: IEEE Computer Society Press

Full text available:  pdf(889.64 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

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IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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2004 Page(s):0_1 - 860
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 2. IEEE standard test access port and boundary-scan architecture
[IEEE Std 1149.1-2001](#)
2001 Page(s):i - 200
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 3. IEEE standard for VHDL waveform and vector exchange to support design and test verification language reference manual
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